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PTO/SB/08A (08-03)

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Use as many sheets as necessary)

Complete if Known

Application Number	10/672,442
Filing Date	September 26, 2003
First Named Inventor	Aladahalli, et al.
Art Unit	2121
Examiner Name	Not Yet Assigned
Attorney Docket Number	DB001050-001

Sheet 1 of 1

U. S. PATENT DOCUMENTS

Examiner Initials*	Cite No. ¹	Document Number	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Number-Kind Code ² (if known)			
JH		US- 6,185,724 B1	02-06-2001	Ochotta	
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FOREIGN PATENT DOCUMENTS

Examiner Initials*	Cite No. ¹	Foreign Patent Document	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages Or Relevant Figures Appear	T ⁶
		Country Code ³ -Number ⁴ -Kind Code ⁵ (if known)				

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Application Number	10/672,442
Filing Date	26 September 2003
First Named Inventor	Aladahalli, et al.
Art Unit	2121
Examiner Name	Not Yet Assigned
Attorney Docket Number	DB001050-001

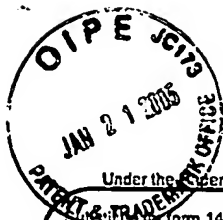
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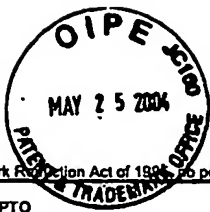
INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Use as many sheets as necessary)		Complete if Known	
		Application Number	10/672,442
		Filing Date	26 September 2003
		First Named Inventor	Aladahalli, et al.
		Art Unit	2121
		Examiner Name	Not Yet Assigned
Sheet 2	of 2	Attorney Docket Number	DB001050-001

NON PATENT LITERATURE DOCUMENTS			
Examiner Initials*	Cite No.†	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T²
JH		CHANDANKUMAR ALADAHALLI, ET AL., A Sensitivity-Based Pattern Search Algorithm For 3D Component Layout, Proceedings of the 2002 Design Engineering Technical Conference,	
		DETC-2002/DAC-34123, September 29 - October 2, 2002, pages 1-10, ASME, Montreal, Canada	

Examiner Signature	/Joseph Hirl/ (06/13/2006)	Date Considered	
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**INFORMATION DISCLOSURE
STATEMENT BY APPLICANT**

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NON PATENT LITERATURE DOCUMENTS

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JH	✓	2001 Graduate Student Technical Conference Masters Presentations Schedule, CMU Mechanical Engineering Web Site, 4/20/2001, pg. 1-8	
	✓	J. CAGAN, et al., A survey of computational approaches to three-dimensional layout problems, July 2002, pgs. 597-611, vol. 34, no. 8, Elsevier	
	✓	M. UPTON, et al., Integrated Placement for Mixed Macro Cell and Standard Cell Designs, 1990, IEEE, pg. 32-35	
	✓	J. CAGAN, et al., A simulated annealing-based algorithm using hierarchical models for general three-dimensional component layout, Sept. 1998, pg. 781-790, vol. 30	
		C. ALADAHALLI, et al., A Sensitivity-Based Pattern Search Algorithm for 3D Component Layout, 2002, ASME, pg.839-848, vol. 2	
		S. KATKOORI, et al., RT-level Interconnect Optimization in DSM Regime, IEEE, April 27, 2000, pgs. 143-148	
		V. TORCZON, et al., From Evolutionary Operation to Parallel Direct Search: Pattern Search Algorithms for Numerical Optimization, Proceedings of the 29th Symposium on the	
↓		Interface, Computer Science and Statistics, May 14, 1997, pgs. 396-401, vol. 29, no. 1	

Examiner Signature	/Joseph Hirl/ (06/13/2006)	Date Considered	
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